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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,641	12/27/2001	Kenneth C. Creta	042390.P12350	9595

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EXAMINER	
CHEN, ALAN S	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,641	CRETA ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Response to Arguments

1. Applicant's arguments filed 12/19/2005 have been fully considered but they are not persuasive.

2. Applicant makes main arguments is that US Pat. No. 6,418,503 to Moertl et al. (Moertl) does not disclose combining a first ordered sequence of transactions and second ordered sequence of transactions into a combined ordered sequence of transactions.

Examiner does not agree. First, nowhere in the independent claims 1, 11, 20 or 23 define exactly what the mechanism is that "combine the first and second ordered sequence of transactions into a combined ordered sequence of transactions" entail. The claims are completely silent as to how exactly the first and second ordered sequences are combined. Any form of multiplexing, interleaving, and even what applicant attempts to argue on pg. 10 of his remarks regarding arbitration, can be construed to be the mechanism in combining ordered sequences.

As stated in the Office Action submitted 08/19/2005, Moertl discloses an ordered sequences of transactions based on the PCI standard. Since there are multiple devices, each generating a transaction (Examiner noted in the previous office action that CPUs 101 and 105 generating the transactions, but it can be the various nodes on PCI buses 1-8, shown in Fig. 1, elements 121-128), there are correspondingly first, second, third, etc., ordered sequence transactions per every node/device. In particular, what creates these ordered sequences are the ***types*** of transactions associated each

transaction. As stated in Column 6, lines 1-15 of Moertl, some transaction types include: Delayed Read Requests (DRR), Delayed Write Requests (DWR), Delayed Read Completions (DRC), and Delayed Write Completions (DWC). Column 8, lines 1-15 give more transaction types, i.e., Post Memory Write (PMW) and PRE or NPRE for prefetchable or non-prefetchable transactions. As shown in Fig. 6, these transaction types intrinsically give "ordering" whenever they are invoked, because these transactions are ultimately reordered for efficiency (Column 3, lines 60-65, to prevent deadlocks and provide fair access to various nodes sharing the primary bus, element 115) by the router. Fig. 7 is an example of ordering performed by the PCI-to-PCI router based on transaction type (steps 719 and 727).

Thus, every node/device generates an "ordered sequence of transactions" based on the transaction type dictated by the PCI standard. These transactions from the various nodes/devices (Fig. 1, elements 121-128, 101 or 105) are effectively "combined" since they share one single bus going into the heart of the PCI to PCI Router (Fig. 3, bolded bus and the Primary PCI Bus, element 115, shown in Fig. 1) and the nodes/devices must arbitrate for the bus (Fig. 3, elements 309 and 321-328). The applicant argues that this arbitration actually teaches away from the invention since Moertl teaches using a "round-robin arbitration scheme". Examiner does not agree, simply due to the vagueness of the claim language. The ordered transactions of each node/device are transmitted over a single bus, thus all the transactions are alternatingly combined via arbitration in order to communicate over a single shared bus. Furthermore, the claim language does not require the ordered sequence to be

numerically ordered, priority based ordered, etc, it simply requires some type of ordering that is met by the intrinsic ordering of the transactions types (Fig. 6 shows ordering at the buffer/queue based on transaction type).

Examiner's rejection is maintained and reiterated below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-6 and 11-27 are rejected under 35 USC 103(a) as being unpatentable over Moertl.

7. As per claims 1, 11, 20 and 23, Moertl discloses a computer chipset, apparatus and I/O hub (Fig. 3) comprising: a port (Fig. 3, element 300) configured to receive first and second ordered sequences of transactions from first and second devices (Fig. 1, elements 101, 105, etc., that are located on a bus 103 sends read/write requests for data over buses 121-128, Column 3, lines 46+, whereupon transactions operated over Fig. 1, element 113 will have transaction ordering since it operates between two PCI buses 103 and 115, pgs. 512-516, of *PCI and PCI Hardware and software Architecture and Design*, hereafter PCI, paying particular attention to pg. 514 where PCI/PCI bridge between two PCI bus segments *must* support Bus Transaction Ordering), wherein the first and second ordered sequences are combined into an ordered sequence of transactions (sequence identifier are intrinsically part of PCI transaction ordering, Moertl discloses the different transaction types in Column 8, lines 3+ and Fig. 6 indicate the ordering scheme by Moertl, these ordered transactions being requests sent over the bus 115 in via arbitration to the router 117, since the bus 115 only allows one transaction at a time, Column 3, lines 55-65); and a router to separate the combined order sequence (the transactions received over bus 115 are received over interface Fig. 3, element 300 and separated by router 305, Column 5, lines 32-55) into two ordered queues based on sequence identifiers associated with the transaction (Column 9, lines

19+, two buffers allow transactions buffer reordering based on the type of transaction coming into the buffer according to reordering rules of Fig. 6). Moertl further discloses PCI-to-PCI bridges, e.g., Fig. 1, element 113, supporting and recognizing requests for various types of transactions, e.g., PMW, DRR, DWR, DWC type transactions and organizing these transactions into separate types of buffers (Column 6, lines 1-15).

Moertl does not disclose expressly an identifier module adding the sequence identifiers (e.g., labeling transaction PMW, DRR, DWR, DWC, etc), however does indicate each transaction will be recognized as a particular type of transaction (Fig. 7, elements 719 and 727).

At the time of the invention it would have been obvious to a person of ordinary skill in the art the need to differentiate the different types of transactions, the simplest design choice being an identification along with the transaction.

The suggestion/motivation for doing so would have been the need to get a handle on each transaction for the purpose of ordering the transactions by the ordering rules of Fig. 6.

Therefore, it would have been obvious to that each transaction have a label/identification as to what type of transaction it since it is a requirement that each transaction by be ordered by the type of the transaction.

8. As per claims 2, 12, 22, 26 and 27, Moertl discloses claims 1, 11, 21 and 23, further comprising an output port (Fig. 3, elements 121 or 128) configured to send the transactions in the two ordered queues (buffers in router 305, shown in Fig. 4) to a data bus (PCI buses 1-8).

9. As per claims 3 and 13-17, Moertl discloses claims 1 and 11, which the first and second sequences are transactions from input/output device (Fig. 1, PCI buses 1-8 are intrinisically designed for expansion, e.g., slots for I/O cards).

10. As per claims 4 and 6, Moertl discloses claim 3, wherein the transactions are read and write transactions (Column 8, lines 3-10).

11. As per claims 5, 18, 19, 21, 24 and 25, Moertl discloses claims 4, 20 and 23, wherein the sequences observe PCI ordering rules (Fig. 6 shows PCI ordering rules).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
03/03/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
3/3/06